LISTING OF THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

1. (Original) A cell structure of non-volatile memory device using a nitride layer as a floating gate spacer comprising:

a gate stack including,

a first portion of a floating gate formed over a semiconductor substrate,

a control gate formed over at least part of the first portion of the floating gate, and

an exposed non-nitride spacer adjacent to sidewalls of the first portion of the floating gate; and

a floating gate transistor including,

a second portion of the floating gate formed over the semiconductor substrate to substantially overlap a portion of at least one of a source and drain implanted in the semiconductor substrate.

2. (Original) The cell structure of claim 1, wherein the gate stack further includes,

an insulating pattern including a nitride layer between the control gate and the first portion of the floating gate.

3. (Original) The cell structure of claim 1, wherein the floating gate transistor further includes,

a nitride spacer adjacent to sidewalls of the second portion of the floating gate

4. (Original) The cell structure of claim 1, wherein the non-nitride spacer includes a polysilicon layer and an oxide layer.

5. (Original) The cell structure of claim 1, further comprising:

a nitride spacer adjacent to sidewalls of the control gate.

6. (Original) The cell structure of claim 1, wherein the first and second portions of the floating gate comprise a polysilicon doped with impurity ions.

7. (Original) The cell structure of claim 1, further comprising:

an insulating pattern of the gate stack formed between the second portion of the floating gate and the semiconductor substrate, the insulating pattern including at least one of an oxide-nitride-oxide (ONO) layer and a nitride-oxide (NO) layer.

8. (Original) The structure of claim 1, wherein the control gate includes a polysilicon layer doped with impurity ions and a silicide layer, and a silicide layer is formed on the source and drain.

9. (Original) The cell structure of claim 1, wherein the non-volatile memory device is at least one of an erasable programmable read-only memory device (EPROM) and a flash memory device.

10. (Original) The cell structure of claim 1, wherein the at least one of an implanted source and drain is operable to inject charges into the first portion of the floating gate in response to a first voltage being applied to the control gate and a second voltage being applied to the second portion of the floating gate, thereby programming a corresponding cell of the non-volatile memory device.

11. (Original) The cell structure of claim 8, wherein the first portion of the floating gate is operable to discharge the injected charges to the at least one of an implanted source and drain in response to ultraviolet rays being applied to the exposed non-nitride spacer of the gate stack, thereby erasing the programmed cell.

12 - 24. (Withdrawn)

25. (Previously Presented) A non-volatile memory whose cell structure is manufactured according to the method of claim 12, wherein the cell structure uses a nitride layer as the floating gate, the cell structure comprising:

the gate stack region further including,

the first portion of the floating gate formed over the semiconductor substrate,

the control gate formed over at least part of the first portion of the floating gate, and

an exposed non-nitride spacer adjacent to sidewalls of the first portion of the floating gate; and

the floating gate transistor region further including,

the second portion of the floating gate formed over the semiconductor substrate to substantially overlap a portion of at least one of a source and drain implanted in the semiconductor substrate.

26. (Original) A non-volatile memory including:

a floating gate formed over a semiconductor substrate;

a non-nitride spacer adjacent to a first portion of the floating gate; and

a nitride spacer adjacent to a second portion of the floating gate, the second portion substantially overlapping at least one of a source and drain in the semiconductor substrate.

27. (Original) The non-volatile memory of claim 26, further comprising:

a control gate formed over the first portion of the floating gate.

28. (Original) The non-volatile memory of claim 27, wherein the at least one of the source and drain is operable to inject charges into the floating gate via hot carrier injection, thereby programming a cell in the non-volatile memory.

29. (Original) The non-volatile memory of claim 28, wherein

the control gate is operable to receive a first voltage;

at least one of the source, drain, and second portion of the floating gate is operable to receive a second voltage; and

the receiving of the first and second voltages causes the at least one of the source and drain to inject the charges via hot carrier injection.

30. (Previously Presented) The non-volatile memory of claim 26, wherein the first portion of the floating gate is operable to discharge charges in response to ultraviolet rays being applied to at least a portion of the non-nitride spacer, thereby erasing a programmed cell in the non-volatile memory.